Abstract

A novel architecture for a multi-scale programmable logic array (MSA) to be used in the design of complex digital systems allows digital logic to be programmed using both small-scale blocks (also called gate level blocks) as well as medium scale blocks (also called Register Transfer Level or RTL blocks). The MSA concept is based on a bit sliceable Arithmetic Logic Unit (ALU). Each bit-slice may be programmed to perform a basic Boolean logic operation or may be programmed to contribute to higher-level functions that are further programmed by an ALU controller circuit. The ALU controller level in this new approach also allows the primitive logic operations computed at the bit-slice level to be combined to perform complex random logic operations. The data shifting capability of this new programmable logic architecture reduces the complexity of the programmable routing needed to implement shift operations including multiplier arrays. The new array also allows logic variables under program control to dynamically modify the micro-program of each ALU. This technique is called configuration overlay and simplifies the programming of complex arithmetic and random logic functions.

ASI-001   Atty Dkt. 08894/025962